Low-k sol-gel coating for surface planarization at integrated circuit production

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The modern development of capacitor and transistor elements of integrated circuits requires the introduction of new thin-film materials into the microelectronic industry. Thus, to increase the number of transistor structures without changing the technological processes, it is possible to obtain multilevel systems. For those purposes, coatings are required to ensure smoothing of the surface of the finished integrated circuit in order for it to form another integral layer. Such coatings should provide a smoothing of the surface from 1 μm to 100-150 nm, and at the same time, to reduce the time delay in integrated circuits with multi-level systems, to have a low dielectric constant.

The paper presents coatings on the surface of the integrated circuit obtained by the sol-gel method from solutions based on the organic compound of silicon. To ensure the necessary smoothing of the surface, two-layer coatings of a total thickness of about 0.6 μm were obtained. The AFM method established that the obtained coatings make it possible to smooth the surface of the integrated circuit from 1 μm to 150 nm (Fig. 1).

Investigation of the electrophysical properties of the obtained two-layer coatings shows that the average value of the permittivity of the dielectric layer is ε = 1.9, which for this thickness of the dielectric is close to the dielectric constant of thermal silicon dioxide. The value of the leakage current through the resulting coating at a voltage of +5 V is 0.9 nA and is retained in this case when the voltage is increased to +100 V. The TPI results show that the value of the voltage shift of the flat zones is Udf = 1.2 V, which corresponds to a change in the density of the effective charge at the interface, that is a small and admissible value.

Thus, developed sol-gel coatings can be used as an interlayer low-k dielectric in the production of multilevel integrated circuits.

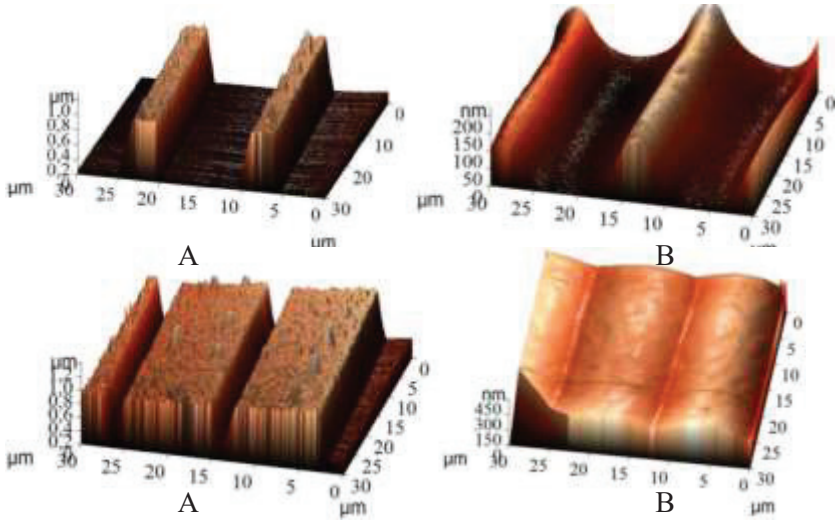

Fig. 1. 3D AFM image (A) without coating, (B) with sol-gel coating

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